

HEVC Hardware Decoder Implementation for UHD Video Applications

Seunghyun Cho, Hyunmi Kim, Kyungjin Byun and Nak-Woong Eum
Multimedia Processor Research Team,
Electronics and Telecommunications Research Institute, Daejeon, Korea
{shcho, chaos0218, kjbyun, nweum}@etri.re.kr

Abstract

In this paper, an efficient hardware architecture that exploits parallel processing for HEVC decoders is proposed by introducing (i) a Coding Tree Unit (CTU)-level pipelined architecture for single-core based processing; and (ii) a multi-core based parallel processing architecture for picture partition decoding with low latency while not requiring additional resources for in-loop filtering (ILF) for neighboring samples of picture partition boundaries. The proposed parallel processing hardware architecture of HEVC decoders is especially effective for UHD video coding where excessive amount of input data inevitably requires a parallel processing architecture for real-time applications. In order to show the effectiveness of the decoder architecture, a dual-core HEVC decoder implementation is tested on a prototyping FPGA board that is available for public demonstration. The decoder design is estimated to be capable of real-time decoding for 4K/8K-UHD bitstreams when implemented on a SoC.

1. Introduction

Recently, the joint collaborative team on video coding (JCT-VC) co-established by ISO/IEC MPEG and ITU-T VCEG, has standardized a next-generation video coding technology called High Efficiency Video Coding (HEVC) [1]. HEVC greatly improved its coding efficiency over its predecessor (H.264/AVC) by a factor of almost 2 times while maintaining equivalent subjective visual quality [2]. Since HEVC has been designed based on large and flexible coding block structures with many advanced coding tools, it is more effective than previous video standards in improving coding efficiency for pictures of higher spatial resolutions such as UHD video [2]. HEVC is well-suited to satisfy the requirements of beyond-HD

video services such as UHDTVs where increased data size requires more efficient data compression.

There has been early effort to implement high performance HEVC hardware decoders [3]-[4]. Our previous work in [3] introduced a single-core HEVC decoder implementation with a 7-stage pipeline architecture. More recently, Huang et al. [4] presented a single-core HEVC decoder chip for 4K-UHD. The decoder in [4] employed a 6-stage interleaved pipeline architecture with variable-size pipeline blocks (VPB), where sample-adaptive offset (SAO) filtering was not implemented. Both HEVC hardware decoders in [3] and [4] were single-core decoders developed in the early stages of HEVC standardization. Although these previous works showed the feasibility of single-core based hardware decoder implementation for the new video coding standard, any study on the multi-core based implementation of parallel processing HEVC hardware decoders has not been presented yet. In this paper, we present a pipeline structure for single-core HEVC hardware decoders based on HEVC Test Model (HM) version 11.0 [5], which is extended to a multi-core based parallel processing architecture with performance scalability for 4K/8K-UHD video applications.

2. Parallel processing architectures for HEVC hardware decoders

2.1. CTU-level parallel processing

One of the most distinguishing features of HEVC is the quadtree coding structure. In HEVC, a Coding Tree Unit corresponds to an array of 64×64 pixels in maximum and contains hierarchical syntax structures needed for decoding the pixels [1]. A picture or one picture partition is partitioned into the CTUs. Thus, it is very straightforward to have a CTU-level pipeline structure for HEVC decoder implementation. If the processing unit block (PUB) for decoder pipeline is a

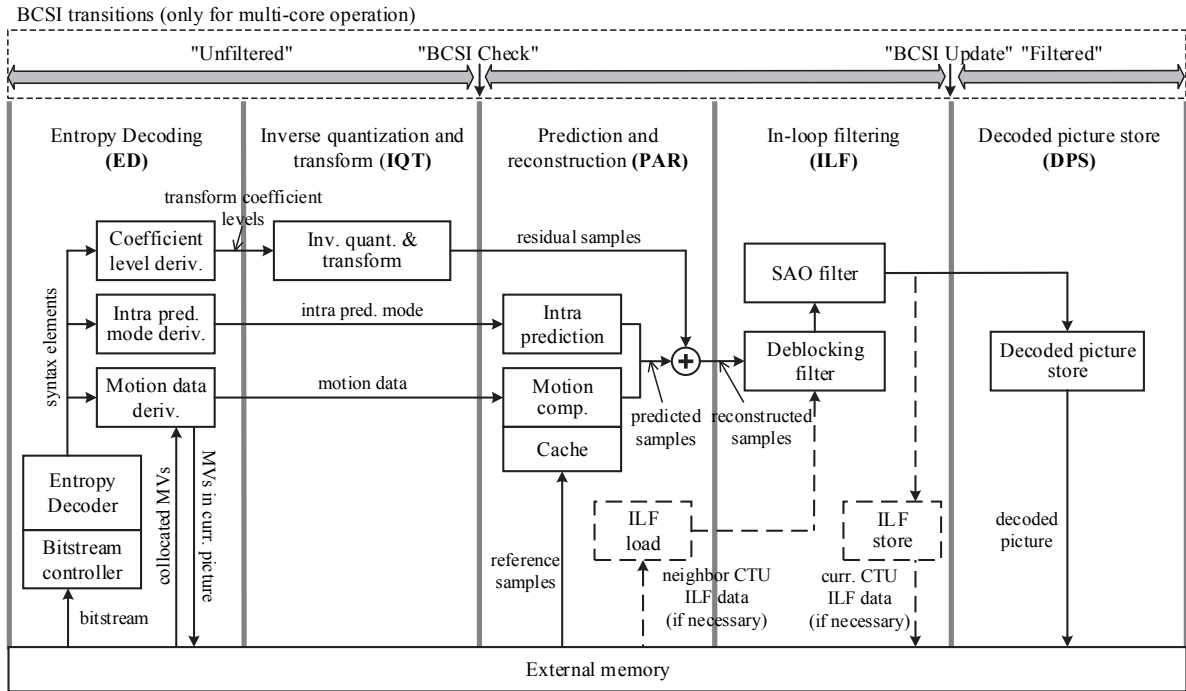


Figure 1. Proposed CTU-level pipeline structure for a single-core HEVC hardware decoder

coding unit (CU), synchronization for decoder pipeline processing becomes difficult because the CUs in a CTU can be partitioned in variable sizes from 8×8 to 64×64 , depending on the signal characteristics of input sequences. Furthermore, since the prediction unit (PU) and transform unit (TU) in HEVC can also be of variable sizes and have data dependency, the PU and TU are more problematic PUBs for decoder pipeline. Therefore, a CTU-level pipeline structure is more appropriate for HEVC decoder implementation.

Figure 1 depicts a CTU-level pipeline structure for a single-core HEVC hardware decoder. The pipeline has with five stages: entropy decoding, inverse quantization and transform, prediction and reconstruction, in-loop filtering, and decoded picture store. In Figure 1, the functional units of the HEVC decoding process are depicted in boxes and data flow is indicated between functional unit blocks by arrows where the input data to a pipeline stage comes from the previous stage or earlier stages.

Motion compensation (MC) module that is mainly composed of a cache and interpolation filters is sub-pipelined with variable-sized MC processing blocks whose maximum size is 16×16 . 81.7% of SRAM between the cache and interpolation filters is saved compared to when the MC module is not sub-pipelined and 30.5% of MC operating cycles are saved compared

to when the MC module is sub-pipelined with 8×8 maximum block size.

2.2. Picture partition-level parallel processing

The performance of an HEVC decoder can be improved by further exploiting the data level parallelism in decoding picture partitions. Picture partitions configured by an HEVC encoder can be independently decoded by a multiple number of single-core decoders with our proposed CTU-level pipeline structure except for the ILF on the neighboring samples of each picture partition boundary (PPB).

In order to design the ILF without additional in-loop filters and synchronizations among decoder cores in a multi-core based HEVC decoder, a boundary CTU status index (BCSI) is defined. The BCSI is a two-bit index indicating the pipeline processing status of a CTU_{PPB} which is adjacent to one or more PPBs. Pixel areas inside and around the current CTU in a PPB can be determined for in-loop filtering along the PPBs by checking one or more BCSIs of the neighboring CTBs in other PPBs. The BCSI of a CTU_{TB} is checked and updated while the CTU_{PPB} is processed in the decoder pipeline shown in Figure 1. Decoder pipeline stall is occurred in a decoder core only when two decoder cores are processing PAR or ILF stages for adjacent CTUs in different picture partitions.

3. FPGA prototyping of multi-core HEVC hardware decoder implementation

The proposed parallel processing architecture is implemented and tested on a FPGA prototyping board for single, dual, and quad cores. A Xilinx Virtex-7 FPGA XC7V2000T is used to implement the multi-core HEVC decoders along with other hardware modules. A 32-bit general purpose RISC is used to parse HEVC high-level syntaxes and control the decoder cores. Once the decoder control registers are set by the RISC, all of the remaining parsing and decoding process is performed by decoder cores in the multi-core HEVC decoder without any CPU intervention. A 2 GB DDR3 SDRAM is used to store bitstream, collocated motion vectors, ILF data and decoded pictures. A video controller is implemented to transfer decoded pictures to an external HDMI-1.4 transmitter for displaying them on a 4K-UHD LCD monitor. AMBA Network Interconnect (NIC-301) is used for the system bus infrastructure of the multi-core HEVC decoder system; A 128-bit AXI bus is used for main video data bus of the decoder system. The implemented HEVC decoder is estimated to be capable of decoding 2160p60 with dual cores operating at 400 MHz or quad cores operating at 200 MHz. An Online

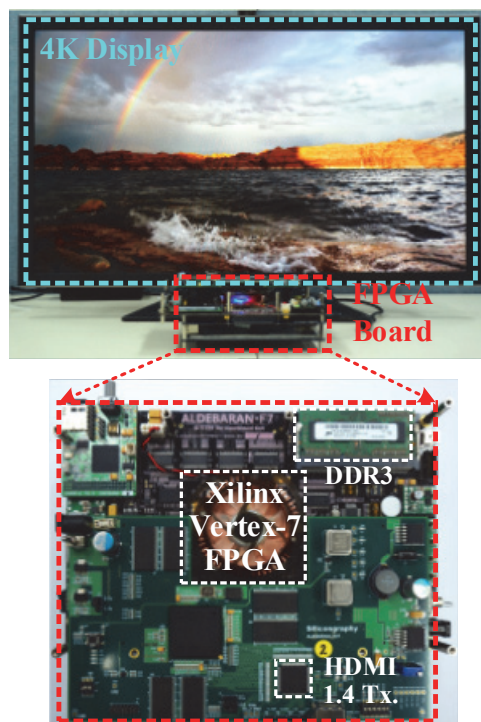


Figure 2. Snapshots of 4K-UHD HEVC decoder demonstration system

video of the decoder demonstration is available at http://youtu.be/ZC_SAww9SoU.

4. Conclusion

In this paper, five-stage CTU-level parallel processing for single-core and picture partition-level parallel processing for multi-core is introduced for 4K/8K-UHD high-performance HEVC hardware decoder implementation. Variable-sized block processing is employed for MC in each core to save both internal SRAM and MC operating cycles. In-loop filtering for samples adjacent to picture partition boundaries is processed without extra in-loop filters using a CTU status management scheme. The proposed decoder architecture is implemented on a FPGA prototyping board and tested for single-, dual- and quad-core operations. Our multi-core decoder design is estimated to be suitable for 4K-8K-UHD real-time decoding of HEVC bitstreams when implemented on a SoC.

5. Acknowledgement

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6. References

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